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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/037,909 | 11/09/2001 | Young-wan Kim | 8021-76 (SS-15501-US) | 6908 |

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| EXAMINER | |
|---|---|
| TRIMMINGS, JOHN P | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | |

DATE MAILED: 06/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/037,909 | KIM, YOUNG-WAN | |
| | Examiner | Art Unit | |
| | John P Trimmings | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-19 are presented for examination.

### *Priority*

The examiner acknowledges the applicants claim for foreign priority or 02/28/2001.

### *Specification*

1. The abstract of the disclosure is objected to because the number of words is 218, but it should contain 150 or fewer words. Correction is required. See MPEP § 608.01(b).

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 10-19 recites the limitation "The error detecting circuit" in the first line. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gervais, U.S. Patent No. 5448725, and in view of Byers et al., U.S. Patent No. 5596716.

As per Claims 1, 9 and 10:

Gervais teaches an error detecting circuit (see Title) comprising: an error data storing unit (FIG.3 210) for dividing a circuit implemented in a chip into predetermined areas (FIG.2 100a...100n), and outputting a plurality of error signals in response to a plurality of state error signals (FIG.2 110a...110n), a lock-enable signal (FIG.3 250 LOCK_ENABLE), and a chip error signal (FIG.3 300 SET_INTERRUPT), each of the plurality of state error signals being enabled (FIG.3 280 ERROR_LOCK) when an error occurs in a corresponding predetermined area (FIG.3 ERROR_INDICATOR1), and the lock-enable signal for determining whether or not to preserve the plurality of state error signals (column 3 lines 58-68 and column 4 lines 1-6); and an error data collecting unit for outputting the chip error signal (FIG.3 290) in response to the plurality of error signals output from the error data storing unit (FIG.3 220 ERROR1_PULSE...ERRORX_PULSE), wherein the error data storing unit stores and outputs at least one of the plurality of state error signals (FIG.3 320 ERROR_INTERRUPT). However, Gervais fails to teach a serial chain signal, the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order when the error occurs in the circuit, and, in response

to the serial chain signal, enables confirmation of at least one of the plurality of state error signals stored in the error data storing unit. In an analogous art, Byers et al. does teach this feature of a serial scan chain signal. In FIG.3 of Byers et al., a serial scan chain composed of a plurality of scan latches, holding collected errors, is scanned out, confirming the state of the stored errors (column 9 lines 49-61 and column 11 lines 10-18). One with ordinary skill in the art would find it obvious that a scan chain would require a scan enable signal in order to scan out a serial scan chain, even though the art did not specifically cite such a signal. And Byers et al., in column 4 lines 21-25 states the advantage of a providing a method and apparatus for identifying and indicating faults in a system during normal operation of the system. One with ordinary skill in the art at the time of the invention, motivated as suggested by the advantage cited, would have found it obvious to combine a scan chain as taught by Byers et al. to store errors in the error storage device of Gervais in order to provide for external viewing of the errors, thus the claims are rejected.

As per Claims 2 and 13:

Gervais further teaches the error detecting circuit of claim 1 or 9, wherein the error data storing unit comprises a plurality of error data registers (FIG.2 110a...110n), each of the plurality of error data registers comprising: a first error data register for outputting a first error signal (FIG.3 220) in response to a first state error signal (FIG.3 ERROR_INDICATOR1), the lock-enable signal (FIG.3 250 LOCK_ENABLE) and the chip error signal (FIG.3 300 SET_INTERRUPT); second through (N-1)-th error data registers for respectively outputting second

through (N-1)-th error signals in response to second through (N-1)-th state error signals, and an N-th error data register for outputting an N-th error signal (FIG.2 ERROR2_PULSE...ERRORn_PULSE) in response to an N-th state error signal (FIG.2 100a..100n), the lock-enable signal (FIG.3 250 LOCK_ENABLE), the chip error signal (FIG.3 300 SET_INTERRUPT), wherein the first state error signal, the second through (N-1)-th state error signals, and the N-th state error signal are comprised in the plurality of state error signals (column 2 lines 5-17). Gervais again does not teach outputting error signals in response to the serial chain signal, and the (N-1)-th error signal. In the analogous art of Byers et al., the feature is taught wherein a serial scan chain composed of a plurality of scan latches, holding collected errors, is scanned out (column 9 lines 49-61 and column 11 lines 10-18). One with ordinary skill in the art would find it obvious that a scan chain would require a scan enable signal in order to scan out a serial scan chain, even though the referenced art did not specifically cite such a signal. Also, it would have been well known in the art and obvious that scanning out of the nth latch would require looking at the output signal of the (n-1)th error. And in view of the motivation to combine for Byers et al. stated in Claim 1 or 9 above, the claims are rejected.

As per Claims 3 and 14:

Gervais further teaches the error detecting circuit of claims 2 or 13, wherein the first error data register comprises: a NAND gate (FIG.3 260 AND in combination with NOT input to 230) for outputting a control signal in response to the lock-enable signal (FIG.3 LOCK_ENABLE 250) and the chip error signal

(FIG.3 SET_INTERRUPT 300), but fails to teach a multiplexer for selecting one of the first error signal or the first state error signal in response to the serial chain signal and the control signal; and a D flip-flop having an input terminal for receiving an output signal of the multiplexer and an output terminal for outputting the first error signal. In the analogous art of Byers et al., this feature is cited in column 8 lines 53-68 and column 9 lines 1-7, but does not specify a multiplexer. A multiplexer in a scan chain however is well known in the art, where the multiplexer is used to select between shift data within the scan chain and the data input. And in view of the motivation to combine for Byers et al. stated in Claims 1 or 9 above, the claims are rejected.

As per Claims 4 and 15:

Gervais further teaches the error detecting circuit of claims 3 or 14, wherein the output terminal of the D flip-flop is a positive output terminal (FIG.3 21 ERROR1_CAPTURE).

As per Claims 5 and 16:

Gervais further teaches the error detecting circuit of claims 2 or 13, wherein any one of the second through (N-1)-th error data registers comprises: a NAND gate for outputting a control signal (ERROR_LOCK NOT input to FIG.3 230) in response to the lock-enable signal (FIG.3 250 LOCK_ENABLE) and the chip error signal (FIG.3 300 SET_INTERRUPT), but does not teach a multiplexer for selecting one of the first error signal, the second error signal and the second state error signal, in response to the serial chain signal and the control signal; and a D flip-flop having an input terminal for receiving an output signal of the

multiplexer and an output terminal for outputting the second error signal. In the analogous art of Byers et al., these features are taught in column 8 lines 53-68 and column 9 lines 1-7, but the reference does not specify a multiplexer. A multiplexer in a scan chain however is well known in the art, where the multiplexer is used to select between shift data within the scan chain and the data input. And in view of the motivation to combine for Byers et al. stated in Claims 1 or 9 above, the claims are rejected.

As per Claims 6 and 17:

Gervais further teaches the error detecting circuit of claim 5 or 16, wherein the output terminal of the D flip-flop is a positive output terminal (FIG.3 21 ERROR1_CAPTURE).

As per Claims 7 and 18:

Gervais further teaches the error detecting circuit of claims 2 and 13, wherein the N-th error data register (FIG.2 110n) comprises: a NAND gate for outputting an N-th control signal (FIG.3 280 ERROR_LOCK NOT input to 230) in response to the lock-enable signal (FIG.3 LOCK_ENABLE 250) and the chip error signal (FIG.3 SET_INTERRUPT 300), nut does not teach a multiplexer for selecting one of the (N-1)-th error signal, the N-th error signal and the N-th state error signal in response to the serial chain signal and the N-th control signal; and a D flip-flop having an input terminal for receiving an output signal of the multiplexer and an output terminal for outputting the N-th error signal. In an analogous art, Byers et al. does teach this in column 8 lines 53-68 and column 9 lines 1-7, but the reference does not specify a multiplexer. A multiplexer in a scan

chain however is well known in the art, where the multiplexer is used to select between shift data within the scan chain and the data input. And in view of the motivation to combine for Byers et al. stated in Claims 1 or 9 above, the claims are rejected.

As per Claims 8 and 19:

Gervais further teaches the error detecting circuit of claims 5 or 18, wherein the output terminal of the D flip-flop is a positive output terminal (FIG.3 21 ERROR1_CAPTURE)

As for Claim 11:

Byers et al. further teaches the error detecting circuit of claim 9, wherein the error data storing unit outputs the at least one of the plurality of state error signals during an abnormal operation in which the chip goes out of order, in response to the serial chain signal (column 8 lines 53-68 and column 9 lines 1-7).

As for Claim 12:

Byers et al. Further teaches the error detecting circuit of claim 11, wherein the serial chain signal is provided externally with respect to the chip (column 9 lines 49-61), where scanning out is controlled by the outside support controller (FIG.4 141).

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number

is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Guy J. Lamarre
for
Albert DeCady
Primary Examiner